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06EC63

Sixth Semester B.E. Degree Examination, June/July 2011
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer FIVE full questions selecting at least TWO questions from each part.***
2. Missing data may be suitably assumed.

PART – A

1 a. Explain the characteristics of a sample and hold circuit used in converting analog signals to digital signals. **(06 Marks)**

b. Determine the maximum DNL (in LSBs) for a 3-bit DAC which has the following characteristics. Does the DAC have 3-bit accuracy? If not, what is the resolution of the DAC having this characteristic? **(05 Marks)**

Digital Input	000	001	010	011	100	101	110	111
Voltage output in V	0	0.625	1.5625	2.0	2.5	3.125	3.4375	4.375

c. Explain in detail the issues in mixed signal layouts with reference to:
i) floor planning ii) power supply and grounding issues iii) shielding. **(09 Marks)**

2 a. Explain charge scaling DACs and layout considerations for a binary weighted capacitor array. **(08 Marks)**

b. A 3-bit resistor string DAC was designed with a desired resister of 500 Ω. After fabrication, mismatch caused the actual value of the resistors to be,
$R_1 = 500\Omega$, $R_2 = 480\Omega$, $R_3 = 470\Omega$, $R_4 = 520\Omega$, $R_5 = 510\Omega$, $R_6 = 490\Omega$,
$R_7 = 530\Omega$ and $R_8 = 500\Omega$.
Determine the maximum INL and DNL for the DAC assuming $V_{ref} = 5$ V. **(06 Marks)**

c. For a binary weighted current steering DAC, obtain the expression for $|INL|_{max}$ and $|DNL|_{max}$ **(06 Marks)**

3 a. With a neat block diagram, explain the successive approximation ADC. Draw the relevant binary search waveform for a 3-bit with D = 101. **(08 Marks)**

b. Design a 3-bit flash ADC with its quantization error centered about zero LSBs. Determine the worst-case DNL and INL, if resistor matching is known to be 5%. Assume that $V_{ref} = 5V$. **(06 Marks)**

c. Explain with a block diagram, dual slope integrated ADC. **(06 Marks)**

4 a. With a relevant diagram using MOSFETs, explain the 3-stages of a voltage comparator. **(12 Marks)**

b. Explain the concept of analog multiplier. With relevant diagram describe the warping of a CMOS multiplier that uses multiplying quad. **(08 Marks)**

PART – B

5 a. Assuming rms quantization noise voltage to be $V_{LSB}/\sqrt{12}$. Show that averaging the outputs of a data converter will improve SNR. **(05 Marks)**

b. Explain the accumulate and dump circuit used for decimation in ADC. Draw the frequency response of the circuit for various values of K. **(10 Marks)**

c. Describe the bandpass filter implementation using a comb filter and a digital resonator. **(05 Marks)**

6 a. With a neat diagram, explain the CMOS process flow for sub – 0.35μm process. **(07 Marks)**

b. Describe the method of implementation of a floating MOS capacitor. **(06 Marks)**

c. Explain how a simple delay element can be realized using i) pass transistor and ii) clock CMOS logic. **(07 Marks)**

7 a. With a neat circuit, explain the working of a 4-bit pipelined adder. Draw the circuit used for implementing 1-bit full adder. **(10 Marks)**

b. Describe the implementation of a switch using NMOS and PMOS logic. **(06 Marks)**

c. Explain the procedures for selecting the channel length of a MOSFET, in analog circuit design. **(04 Marks)**

8 a. Explain the process of biasing a push-pull amplifier o/p stage with a floating current design. **(05 Marks)**

b. Describe the operation of differential amplifier that uses source follower level shifter for boosting OP-AMP gain. **(07 Marks)**

c. Describe a mixed signal OP-AMP topology. **(08 Marks)**

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